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09/346,436	07/01/1999	THEODORE W. HOUSTON	TI-21004	2434

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	18

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/346,436	Applicant(s) Houston
	Examiner Erik Kielin	Art Unit 2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 18, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-4, 7-9, and 18-26* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-4, 7-9, and 18-24* is/are rejected.

7) ☒ Claim(s) *25 and 26* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

1. In view of the Reply Brief filed on 10/18/01, PROSECUTION IS HEREBY REOPENED. A rebuttal to the Reply Brief is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(a) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(b) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

The Reply Brief filed 10/18/01 presents **new arguments** not presented in the Appeal Brief which warrant rebuttal -- especially since no arguments concerning claims at issue (9 and 22) were originally presented. Instead, only allegation that the features claimed in Applicant's claims 9 and 22 were absent in the applied prior art reference of Hayashi. (See the last paragraph on each of pages 6 and 7 of the Appeal Brief.)

Note that 37 CFR 1.192(c)(7) (1995) states,

> "For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. **Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.**" (Emphasis added.)

Inasmuch as Appellant only points out the differences in "what the claims cover" (at the location of the Appeal Brief noted above), there constructively exists no argument as to why the claims 9 and 22 stand alone. Accordingly, the claims 9 and 22 should stand or fall together with the independent claims, 7 and 18 respectively, from which each depends. Since claims 7 and 18 were withdrawn from appeal in the Reply Brief, so should be claims 9 and 22.

If it is thought that the claims 9 and 22 do not stand or fall together with their independent claims 7 and 18, respectively, then the following rebuttal to the new arguments presented in the Reply Brief is presented below.

On page 1 of the Reply Brief, Appellant argues the claim 9 requires the limitation that "the electrical interconnect structure in the electrically insulating layer contact **both** the device layer and the substrate." Appellant then argues,

> "The interconnect structure of Hayashi is the metal pool which does not contact both the device layer and the substrate. This contact is only later made when the refractory metal bump later contacts the metal pool. Accordingly, the order of the steps as specifically claimed in the combination of claims 7 and 9 is not met by Hayashi."

This argument is in error for two reasons. First, the interconnect structure of Hayashi (the metal pool) does, in fact, contact both the substrate and the device layer. Without such contact no electrical connection could exist, therefore contact is made. If it is thought that the refractory metal bump is not part of either the device layer then this may be a difference, but the Hayashi Figures (Fig. 2A for example) clearly show the refractory metal bump to be part of the device layer inasmuch as it is used to electrically interconnect the device layer to the refractory metal pool. If it is thought that the interconnect structure of Hayashi (the metal pool) does *not* contact the substrate because there is another intervening device layer (item 23 in Fig. 2B of Hayashi), then this might be a difference, **but in pertinent point**, Appellant's specification indicates on page 6, lines 6-8, that, "[t]he device wafer 5 and the substrate 1 may have active and/or passive devices formed therein and optionally making a connection to an interconnect in the electrically insulating layer." Therefore, Appellant (1) explicitly defines both the "device wafer" and the "substrate" to include "devices" which is identical to the substrate and device wafer of Hayashi show in Figs. 2A and 2B, as each have devices; and (2) explicitly defines the refractory metal bump to be part of the device layer, by using the phrase, "optionally making a connection to an interconnect in the electrically insulating layer" because the refractory metal bump makes a connection to the "interconnect in the electrically insulating layer." Accordingly, Appellant is in error in indicating that the interconnect structure of Hayashi does not contact both the device wafer and the substrate.

Second, regarding the second and third sentences in the excerpt above, Appellant appears to argue that Appellant's interconnect structure formed in the electrically insulating layer somehow contacts both the device wafer 5 and the substrate layer **prior** to the bonding step. This assertion is in complete contradiction to the clear language of each of the independent claims and the specification. The point of Appellant's invention is to **first** form the "interconnect in the electrically insulating layer" and **then** bond it to the device wafer and/or substrate, **thereby forming electrical connections** thereamongst. Note that the interconnect layer may be formed initially on **either** the device wafer 5 or the substrate (handle wafer) 1 **before** bonding to the other, as clearly stated in claim 1, step (c). Therefore, the argument presently by Appellant is in error because electrical connection of the interconnect layer to **both** the device wafer and the substrate, only occurs **after** bonding -- not before. Note that this is the same order as shown in Hayashi's Figs. 2A-2C --not a different order as alleged by Appellant.

Regarding page 2 of the Reply Brief, Appellant argues,

> "As to claim 22, there is no so-called admission in Appellant's APA that it is even known that the oxide will appear in the process as claimed, let alone that it be known to remove such oxide, especially in the environment claimed."

It is respectfully submitted that this argument is wholly without merit. First, and as pointed out in the rejections and restated here for convenience, Appellant's specification states,

> "In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, **a sufficiently**

> **high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or the other dielectric** and allow completion of the connection **as is well known in the art**." (Emphasis added; specification page 7, lines 7-12.)

Appellant very explicitly states that it is known to remove any oxide forming over the interconnect using a high voltage if it forms. It begs the question as to how one would know to remove the oxide if no oxide were known to be formed in the first place. Therefore, it must be known that the oxide may form; otherwise, one would know to remove it or how to remove it. Regarding the "claimed environment," there is no claimed environment, so this issue is moot. Accordingly, the points at issue in claim 22 is clearly admitted prior art.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1**, 3, 7-9 and **18**-21, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by **Hayashi** (US 5,087,585).

Regarding claims 1 and 3, Hayashi discloses a method of fabricating an SOI structure comprising:

(a) providing a substrate 21 (Fig. 2B) having at least one of active or passive elements on a surface thereof (i.e. the "first layer device" 22);

(b) providing a device wafer 14, 15 having at least one of active or passive elements on a surface thereof (i.e. "second layer thin film device" 23);

(c) forming an electrically insulating layer 17 having opposed faces on the surface of one of the substrate and the device wafer and having an electrical interconnect structure 18 therewithin and extending to at least one face; and

(d) bonding said electrically insulating layer to the substrate at the bond region 13, a refractory metal bump, wherein the interconnect structure 18 contacts the bond region (Figs. 2B-2C).

Note that on page 7, lines 5-7 of Appellant's specification, layer 5 is referred to as the "device layer 5" which is shown only as a layer in Appellant's figures **without** any specific "passive" or "active" elements as claimed. Compare to either of 22 or 23 in Fig. 2B of Hayashi, as noted above, which shows the same nondescript "first layer device" or "second layer thin film device.")

Regarding claims 7-9, Hayashi discloses a method of fabricating an SOI structure comprising:

providing a substrate 21, 22 (Fig. 2B), with a planar surface, having at least one of active or passive elements on a surface thereof (i.e. the "first layer device" 22); a device wafer 14, 15, 23, with a planar surface, having at least one of active or passive elements on a surface thereof

(i.e. "second layer thin film device" 23); and an electrically insulating layer 17 having an electrical interconnect structure 18 therewithin and extending to a surface thereof, said interconnect structure separating a portion of said device layer from said substrate;

Regarding claims 18-21, and 23-24, Hayashi discloses a method of fabricating an integrated circuit comprising:

(a) providing a device layer 23 having devices (Fig. 2B);

(b) providing a substrate 21 having devices 22 thereon;

(c) providing a dielectric 17 bonded to one of said device layer and said substrate having an interconnect 18 disposed therein and extending to at least one surface thereof; and

(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate and forming an electrically conductive path across said interface to said interconnect.

See also columns 3-4 and column 5, lines 11-16.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1**-4, 7-9 and **18**-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi** in view of Appellant's admitted prior art (**APA**).

Hayashi, as indicated above, discloses all of the features of the instant invention except for applying a voltage across an electrically insulating layer to break down said portion of said electrically insulating layer.

On page 7, lines 7-12, **Appellant** indicates that it is known in the art to break down oxide by applying voltage across an electrically insulating layer by stating,

> "In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, **a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or the other dielectric** and allow completion of the connection **as is well known in the art.**" (Emphasis added; specification page 7, lines 7-12.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify **Hayashi** by Appellant's **APA** because native oxide (i.e. the electrically insulating layer) inherently forms on all metals (perhaps with the exception of gold) upon exposure to air -- and, in particular, would form on **Hayashi's** refractory metal bump and indium metal pool -- and Appellant admits that it is known in the art for such dielectric to form incidentally, and that it should be removed in order to establish the electrical connection, by the known art means of applying an electrical voltage.

Allowable Subject Matter

6. **Claims 25 and 26** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Although Applicant's specification states that it is "well known in the art" to break down an electrically insulating layer, such as a "thin native oxide" or "flowable dielectric" formed during fabrication of the interconnect, the prior art of record does not teach or suggest *intentionally forming* "an electrical insulation" over the interconnect before bonding the interconnect substrate to the device substrate and then electrically breaking down the "electrical insulation."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rioult (US 3,787,822) teaches applying a voltage across a dielectric interface 16 between conductive metal layers 12, 15 interface to remove native metal oxide from interconnect material (Abstract).

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication from examiner should be directed to Erik Kielin whose telephone number is (703) 306-5980 and e-mail address is erik.kielin@uspto.gov. The examiner can normally be reached by telephone on Monday through Thursday 9:00 AM until 7:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached at (703) 308-2417 or by e-mail at charles.bowers@uspto.gov. The fax phone number for the group is (703) 308-7722 or -7724.

EK

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